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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FUMITOMO MATSUOKA

Appeal 2008-2522
Application 10/779,661
Technology Center 2800

Decided: June 23, 2008

Before ROMULO H. DELMENDO, LINDA M. GAUDETTE, and MICHAEL P. COLAIANNI, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 14, 15, 17, and 18.[1] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] An oral hearing was held on June 10, 2008.

The invention relates to an insulated gate field effect transistor ("MISFET") having a buried-type gate electrode structure. (Spec. 1, ll. 12-14.) Claim 14 is illustrative of the invention and is reproduced below:

14. A semiconductor device comprising:

a semiconductor substrate;

a first impurity diffusion layer formed in the semiconductor substrate;

a second impurity diffusion layer formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer formed on the first impurity diffusion layer so as to cover the first impurity diffusion layer except for a tip portion opposite to the second impurity diffusion layer;

a second insulating layer formed on the second impurity diffusion layer so as to cover the second impurity diffusion layer except for a tip portion opposite to the first impurity diffusion layer;

a trench formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer;

a gate insulating film lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench, the gate electrode conductive layer being formed in an overlapped relation relative to the tip portion of the first impurity diffusion layer and the tip portion of the second impurity diffusion layer,

wherein the gate insulating film contains one selected from the group consisting of Ta_2O5, Al_2O_3, $BaSrTiO_3$, Zr oxide Hf oxide, Sc oxide, Y oxide, and Ti oxide.

The Examiner relies on the following prior art reference to show unpatentability:

Xiang 6,159,782 Dec. 12, 2000 (Aug. 5, 1999)

The Examiner rejected claims 14, 15, 17, and 18 under 35 U.S.C. § 102(e) as anticipated by Xiang.

Appellant argues that the Examiner's rejection is improperly based on a finding that Xiang Figure 12B discloses the claim feature of "the gate electrode conductive layer being formed in an overlapped relation relative to the tip portion of the first impurity diffusion layer and the tip portion of the second impurity diffusion layer" (independent claim 14). (Reply Br. 2.) More specifically, Appellant contends that Xiang's drawings are ambiguous with respect to the positioning of these elements and, therefore, cannot be relied upon to establish anticipation. (*See* App. Br. 4-9.)

Appellant does not present separate arguments for patentability of dependent claims 15, 17, and 18. Therefore, the sole issue presented on appeal is: Has Appellant identified reversible error in the Examiner's finding that Xiang Figure 12B anticipates claim 14 within the meaning of 35 U.S.C. § 102(e)? We answer this question in the negative for the reasons discussed below.

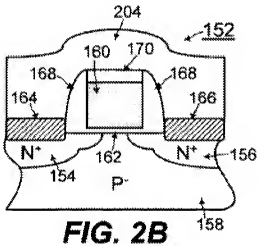
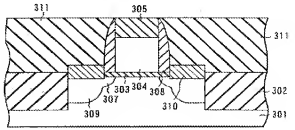
In our view, the Examiner properly established a prima facie showing of anticipation based on the factual findings and analysis set forth in the Answer (Ans. 4-7). The following enumerated findings of fact ("FF")

support the Examiner's finding of anticipation, and are of particular relevance to our consideration of the issue presented in this appeal[2]:

1) Xiang discloses "[a] method for fabricating short channel field effect transistors with dual gates and with a gate dielectric having a high dielectric constant." (Abstract.)

2) Figure 2B of Xiang and Figure 12 of Appellant's Application are shown side-by-side below:

[2] Appellant states that "[t]he subject matter of independent Claim 14 includes a semiconductor device shown in various manufacturing stages in FIGS. 9-15, for example, and as an exemplary insulated gate field effect transistor . . . in FIG. 16, for example." (App. Br. 2.) We are mindful that a proper analysis under 35 U.S.C. § 102(e) requires a comparison of the *claimed* invention to the prior art. We provide comparisons between Xiang's disclosure and Appellant's Specification and Drawings for the limited purpose of illustrating similarities in the semiconductor fabrication methods.

 FIG. 2B Xiang Figure 2B shows an intermediate structure of an NMOSFET 152 during a step in the disclosed method. (Col. 3, ll. 43-48; col. 5, ll. 63-65.)	 FIG. 12 Figure 12 of Appellant's Application shows an intermediate structure of the n-type MISFET during a step in the fabrication of the final structure.
a) The NMOSFET includes a dummy gate electrode 160 comprised of polysilicon, and an optional layer 170 comprised of silicon oxynitride. (Col. 5, ll. 21-22 and 29-32.) b) An SiO_2 layer 162 serves as a sacrificial gate dielectric 162. (Col. 5, ll. 22-23.)	The MISFET includes a dummy gate electrode comprising a polycrystalline silicon film 304 and a silicon nitride film 305. (Spec. 12, ll. 7-10.) SiO_2 film 303 serves as a dummy gate insulating film.

c) A layer of insulator material 204, such as SiO_2, is deposited to surround the dummy gate electrode 160 using a known method. (Col. 5, l. 63 – col. 6, l. l. 3.)	An SiO_2 film, serving as an interlayer insulator 311 is deposited over a whole surface of the structure with the use of a chemical vapor deposition method
d) Spacers 168 comprised of insulator material such as silicon dioxide surround the dummy gate electrode 160. (Col. 5, ll. 27-29.)	A sidewall insulating film 308 is formed of silicon dioxide.
e) During fabrication, the dummy gate electrode 160 and the sacrificial gate dielectric 162 are selectively etched away using known techniques to form a gate opening 214. (Col. 6, ll. 25-29 and 33-36.)	During manufacture, dummy electrode 317 is eliminated by etching. This provides a trench 312. The width of the trench 312 is enlarged by an extent corresponding to the film thickness of a desired gate insulating film. It is desirable to perform an etching at this time such that both the dummy gate insulating film 303 present on the bottom and sidewall insulating film 308 present on the sidewall area of the burying trench are simultaneously etched.

f) The gate opening 214 has side walls of the insulator material from the spacers 168 or the layer of insulator material 204. (Col. 6, ll. 29-31.)	If, in this step, the width of the trench is further enlarged by an etching to an extent exceeding the thickness of the sidewall insulating film 308, even when a thicker gate insulating film is formed at a later step, it is easy to obtain an overlapped structure in which the end of the gate electrode 314 overlaps the extensions 307 of the impurity diffusion layers 309.
g) A layer of dielectric with a high dielectric constant (e.g., Ta_2O_5) is then deposited on the side walls and the bottom wall of the gate opening 214 using a known method such as CVD. (Col. 6, ll. 46-52.) Optionally, a layer of nitrided oxide 224 is deposited on the side walls and bottom wall of the gate opening prior to layer 225. (Col. 6, ll. 52-53.)	Subsequently, a Ta_2O_5 film is deposited, as a desired gate insulating film material, with the use of the chemical vapor deposition method and sputtering method. By doing so, the gate insulating film 313 is deposited on the interlayer insulator 311 and on the exposed inner surface of the trench 312. (Spec. 15, ll. 21-27.)

3) Figure 12B of Xiang and Figure 16 of Appellant's Application are shown side-by-side below:

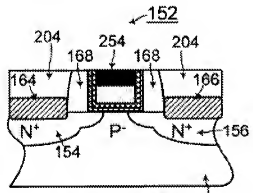


FIG. 12B

Xiang Figure 12B shows the final structure of NMOSFET 152, which may be further coupled to other integrated circuit components. (Col. 9, ll. 26-29.)

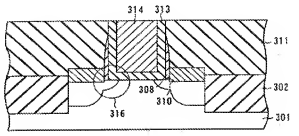


FIG. 16

Figure 16 of Appellant's Application shows the final structure of the n-type MISFET. (Spec. 16, ll. 6-8.)

A reference is anticipatory within the meaning of § 102 if it discloses each and every claim limitation either expressly or inherently. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997). "The anticipation analysis asks solely whether the prior art reference discloses and enables the claimed invention, and not how the prior art characterizes that disclosure or whether alternatives are also disclosed." *Hewlett-Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1324 n.6 (Fed.Cir.2003). Description for the purposes of

anticipation can be by drawings alone as well as by words. *In re Bager*, 47 F.2d 951, 953 (CCPA 1931). "[W]hether an accidental showing in a drawing is or is not an anticipation of a later invention depends generally upon the facts in each particular case." *Id.* at 952-53.

Appellant does not dispute the Examiner's finding that Xiang Figure 12B illustrates a semiconductor device in which the gate electrode conductive layer is formed in an overlapped relation relative to the tip portions of the first and second impurity diffusion layers. (*See* Reply Br. 2.) Rather, Appellant contends that the Xiang drawings, standing alone, do not provide the type of accurate, particular, and precise description required to establish anticipation. (App. Br. 7.) We have considered Appellant's arguments in light of the relevant case law, but are not persuaded of reversible error on the part of the Examiner.

According to Appellant, the relevant case law "establishes it to be erroneous to rely on a drawing illustration of the relative proportions of illustrated elements when the disclosure is devoid of any indication that the proportions of these elements are drawn to scale." (Reply Br. 3; *see* App. Br. 6-7) (citing *Hockerson-Halberstadt, Inc. v. Avia Group, Int'l, Inc.*, 222 F.3d 951 (Fed. Cir. 2000) and cases cited therein). Appellant points out that Xiang specifically states that the figures are not necessarily drawn to scale (App. Br. 6-7; Reply Br. 2-3) and there is no corresponding description in Xiang's specification to support a finding of an actual overlap in the gate electrode and impurity diffusion layers in Xiang's semiconductor device (App. Br. 7-8; Reply Br. 4). Appellant further suggests that the absence of any disclosure as to the purpose of spacers 168 and the method used to form the tips of Xiang's source/drain regions 154, 156 would have led the

ordinary artisan to assume that Xiang's process resulted in a conventional structure in which the spacers 168 were directly over and aligned with the edges of regions 154/156 as shown in Appellant's Specification Figures 1-8, rather than a structure in which spacers 168 overlap regions 154/156 in the manner depicted in Xiang's drawings. (*See* App. Br. 8-9; Reply Br. 4-7). Appellant contends that the ordinary artisan would likewise have concluded that Xiang's illustration of an overlap between the gate electrode conductive layer and the tip portions of the first and second impurity diffusion layers shown in Figure 12B was merely an exaggeration. (Reply Br. 5-7; *see* App. Br. 9).

We do not view the case law relied upon by Appellant as particularly relevant to the facts in this appeal.[3] As pointed out by the Examiner, "this is

[3] *See Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) ("HHI's argument thus hinges on an inference drawn from certain figures about the quantitative relationship between the respective widths of the groove and fins. Under our precedent, however, it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977) (declining to find that, based on a comparison of the relative dimensions of appellant's and patentee's drawing figures, patentee's disclosure "clearly point[ed] to the use of a chime length of roughly 1/2 to 1 inch for a whiskey barrel"); *In re Wilson*, 312 F.2d 449, 454 (CCPA 1963) (noting that specific dimensions could not be established based on measurements of patent drawings); *In re Reynolds*, 443 F.2d 384 (CCPA 1971) (considering the issue of whether drawings supported claim language in an appeal from the Examiner's rejection under 35 U.S.C. § 112, first paragraph); *but see In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972) ("[A]s we said in *Wilson*, supra, 'Patent drawings are not working drawings * * *.' However, we did not mean that things patent drawings show clearly are to be *disregarded*. In re Bager, also cited by appellant, is an example of

not an issue of size or scale but rather the positioning of a region relative to another region." (Ans. 5). We find the facts in the present case are more analogous to those in *Bager*, 47 F.2d 951, and, therefore, are guided by the court's analysis in that case.

In *Bager*, the Appellants argued that the location of a padlock sheave in a shovel, as depicted in the reference drawings, was accidental, and that an accidental showing was not an anticipation. *Id.* at 952.[4] The court disagreed, explaining that an accidental showing in a prior patent may still anticipate a later invention unless

> the thing so shown is not essential to the first invention, and was not designed, adapted, or used to perform the function which it performs in the second invention, and was neither intended nor appreciated by the patentee, and when the first patent contains no suggestion of the way in which the result sought is accomplished by the second inventor.

Id. at 953. Thus, in deciding the appeal, the court assumed that the position of the sheave shown in the reference was not essential to the patentee's invention and was not designed or used to perform the function which it performed in the Appellants' invention. *Id.* The court commented that the Board had correctly identified the relevant inquiry on appeal as "whether one skilled in the art seeing the disclosure of the [reference] would understand that the sheave was to be located in the position there shown and whether, were such a construction built and operated, the advantages

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a case in which the teachings of patent drawings, even as to features unexplained by the specification, proved dispositive.").

[4] In support of their position, Appellants presented affidavits of experts in the field stating that the shovel, as depicted in the drawings, was impractical. *Id.* at 951-52.

claimed to result from such location of the sheave would be secured." *Id.* at 952.[5]

Applying a similar analysis, we view the Xiang disclosure in a light most favorable to Appellant, and assume that the overlap of the gate electrode conductive layer relative to the tip portions of the first and second impurity diffusion layers depicted in Xiang Figure 12B was not essential to the invention and was not necessarily designed or used to perform the function which it performs in Appellant's claimed invention. We then consider whether one of ordinary skill at the time of the invention, seeing Xiang Figure 12B, would have concluded that the gate electrode conductive layer was to be formed in an overlapped relation relative to the tip portions of the first and second impurity diffusion layers, and whether a semiconductor device having this structure would have the advantages of Appellant's claimed device.

Appellant has not convinced us that the ordinary artisan would have assumed that Xiang's illustration of overlapping regions was merely an exaggeration. Xiang discloses a semiconductor in which the gate insulating film is formed from a high dielectric material (FF 1). Contrary to Appellant's contention, we think one of ordinary skill in the art at the time of the invention would have suspected that Xiang's overlapping layer structure provided some advantage over a conventional structure (i.e., a structure in

[5] The court ultimately found "that any person skilled in the art, realizing the desirability of permitting the bucket to be raised to the extreme height permitted by the boom, would, after seeing [patentee's] drawing, position the sheave as appellants have done, and therefore [concluded] that appellants' disclosure, in view of the [] reference, [did] not constitute invention." *Id.* at 953.

which the spacers are aligned with the edges of the source/drain regions) where a high dielectric material, rather than a more conventional material (e.g., silicon oxide) was employed as the gate insulating film (*see* Spec. 1:17 – Spec.3:27 (describing conventional MISFET manufacturing processes)). *Cf. Reynolds*, 443 F.2d at 389 ("[W[e think a person skilled in the art would suspect that there was some reason for the relationships shown in the drawing and would not regard such disclosure as accidental or arbitrary."). Although Xiang does not disclose the specific steps by which the gate opening 214 is formed, Xiang does state that the side walls of the gate opening 214 may be the insulator material from spacers 168 or the layer of insulator material 204 (FF 2f). In our view, one of ordinary skill in the art would have understood from this disclosure that the width of gate opening 214 could be further widened after etching away the dummy gate electrode 160 and the sacrificial gate dielectric 162 (FF 2e), by removing all, or a portion of spacers 168.[6] Therefore, like the Examiner, we are of the opinion that "[t]he only conclusion that one of ordinary skill in the art can make which is definitive and not speculative in nature is that the first and second diffusion regions overlap the gate electrode because it is clearly disclosed in FIG. 12B of Xiang" (Ans. 6). *See In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) (*quoting*, *In re LeGrice*, 301 F.2d 929, 936 (CCPA 1962)) (A reference anticipates a claim if it discloses the claimed invention "such that a

[6] Additionally, we note that Appellant's arguments regarding the understanding of one of ordinary skill in the art lack persuasive merit because they are not supported by appropriate evidence. *See C.R. Bard, Inc. v. Advanced Cardiovascular Sys.*, 911 F.2d 670, 674 n.2, (Fed. Cir. 1990) (attorney arguments are not evidence).

skilled artisan could take its teachings in *combination with his own knowledge of the particular art and be in possession of the invention*.").

In sum, we find that Appellant failed to identify reversible error in the Examiner's finding that Xiang Figure 12B anticipates claim 14 within the meaning of 35 U.S.C. § 102(e).

ORDER

The decision of the Examiner rejecting claims 14, 15, 17, and 18 under 35 U.S.C. § 102(e) as anticipated by Xiang is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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